AMENDMENTS TO THE CLAIMS

1-19. (Canceled).

20. (Currently Amended) A method for fabricating a semiconductor memory element arrangement, comprising the steps of:

forming a first electrically insulating layer on a substrate;

forming a layer system, including a floating gate and a multiple tunnel barrier arrangement formed on the floating gate, on the first electrically insulating layer;

forming a first trench structure in the layer system, the first trench structure having first trenches arranged parallel to one another and extending as far as the first electrically insulating layer;

forming a second trench structure in the layer system, the second trench structure having second trenches arranged parallel to one another and extending as far as the first electrically insulating layer, the second trenches being arranged perpendicular to the first trenches;

forming, in the first and second trench structures, a first gate electrode adjacent to the floating gate through which first gate electrode electrical charge is ~~can be~~ fed or ~~can be~~ dissipated from; and

forming, in the first and second trench structures, a second gate electrode adjacent to the multiple tunnel barrier arrangement, wherein through the second gate electrode an electrical charge transmission of the multiple tunnel barrier arrangement ~~can be~~ is controlled.

21. (Previously Presented) The method as claimed in claim 20, wherein the steps of forming the first and second trench structures comprise the steps of:

forming a second electrically insulating layer on the multiple tunnel barrier arrangement; and